Amendments to the Specification

Please replace the paragraph beginning on page 1, line 4 with the following amended paragraph:

A claim of priority is made to U.S. provisional application Serial No. 60/421,779 ~~10/421,779~~, filed October 25, 2002, the entire contents of which are incorporated herein by reference.

Please replace the paragraph beginning on page 1, line 14 with the following amended paragraph:

Arrays of precision capacitors are used in various switched capacitor circuits. One example is illustrated in Fig. 1, where a switched-capacitor DAC using (n+1) capacitors (C, 2C,...,2^{n-1}C, 2^{n}C) with a common top plate and separate bottom plates is shown. The use of a similar capacitor array of capacitors (C_1=C, [[C_2=C]] $C_2 = 2C$,..., $C_{K+1}=2^{K-1}C$) in an ADC is presented in Fig. 2. In both cases, the values of the capacitances are powers of 2 of a unit capacitance. For matching reasons, the capacitor arrays are built from unit capacitors, interconnected as to provide the appropriate values, and distributed in the array as to compensate for the gradients of the dielectric thickness. In the particular cases shown in Figs. 1 and 2, the top plates of the capacitors of the arrays are common.

Please replace the paragraph beginning on page 6, line 16 with the following amended paragraph:

The basic capacitor according to this disclosure is shown in Fig. 5. The capacitor is built out of a sandwich of three metal plates, in three different metal layers, on an oxide layer 520 formed in substrate 510. Let's assume, for instance, that the metal layers used are Metal1 (Ml), Metal2 (M2) and Metal3 (M3).

Please replace the paragraph beginning on page 6, line 21 through to page 7, line 6 with the following amended paragraph:

The capacitor consists of:

- a top plate 570 made of Metal2 and having an opening 573 in the center and conductive branch members 572;

- a first bottom plate 550 made of Metal1 ;

- a second bottom plate 590 made of Metal3;

- a stack of via 560, ~~Metal2 plate 571~~ Metal2 plate 511 and via 561 connecting the first and the second bottom plates through the 573 opening;

- a contact [[means]] structure 540 connecting the first bottom plate 550 to a bottom connection 530 placed between the first metal plate and the substrate.

Please replace the paragraph beginning on page 8, line 18 through to page 9, line 14 with the following amended paragraph:

Fig. 7 shows an example of using the capacitors of Fig. [[5a]] 5 in an array built according to this invention, with bottom interconnections and common top plate. The array of capacitors includes the capacitors 711, 712, 713, 721, 722, 723, 731, 732, 733, 741, 742, 743, 751, 752, 753, 761, 762, 763 of identical structure and size. As an example, the capacitors can be built with Metal1, Metal2 and Metal3 plates, with bottom interconnections made of polysilicon. The capacitors are arranged in a 6 rows by 3 columns matrix. There are 1+1+2+4+8=16 active capacitors and two dummy capacitors (712 and 762). Each column of capacitors has four bottom interconnection lines: 7101, 7102, 7103, 7104 for the 711,721,..., 761 capacitors; 7201, 7202, 7203, 7204 for the 712, 722,...,762 capacitors; 7301, 7302, 7303, 7304 for the 713, 723,...,763 capacitors. The unit capacitors allocation is as following:

- to the C8 capacitor: 711, 721, 751, 761, 713, 723, 753, 763;
- to the C4 capacitor: 731, 741, 733, 743 ;
- to the C2 capacitor: 722, 752;
- to the C1a capacitor ~~C1acapacitor~~: 732;
- to the C1b capacitor: 742.

Please replace the paragraph beginning on page 9, line 17 with the following amended paragraph:

The bottom plates of the capacitors 711, 721, 751 and 761 belonging to the C8 capacitor are connected through the bottom connection 7102 [[7103]], accessible both from the top and from the bottom of the capacitor array.

Please replace the paragraph beginning on page 11, line 11 through to page 12, line 8 with the following amended paragraph:

Figure 8 shows the internal portion of an array of capacitors fabricated in accordance to the present invention and a cross section of this structure. The middle layer terminal of each capacitor (top capacitor plate) is separated and is denoted in gray. The black center square of each unit capacitor represents the contact between the top and the bottom conductive layers that form the bottom capacitor plate. The whole array is equivalent to a multi-terminal capacitor due to the fact that the unit capacitors are close to each other and the electrical field of one can influence the charges on the neighboring capacitors. The cross section from figure 8 shows the different terminals of this multi-terminal capacitor. If one grounds all terminals except T4, the total capacitance [[ofT4]] of T4 will be the sum of the different mutual capacitances. If we take into consideration a bi-dimensional case and neglect the capacitances related to other terminals except the ones presented in the cross section then:

$C_3=C_{30}+C_{31}+C_{32}+C_{34}+C_{35}+C_{36}$

Where:

C30 is the parasitic capacitance of terminal T4 to ground, C_{mn} is the capacitance between terminal TM and TN where M=1,6 and N=1,6.

Please replace the paragraph beginning on page 12, line 14 through to page 13, line 5 with the following amended paragraph:

The usual way to build a well-balanced and matched array of capacitors is to place at the periphery a border of dummy devices that will compensate for non-uniform etching and other neighboring-related non-idealities. Figure 9 shows the traditional way of connecting dummy capacitors at the periphery of a capacitor array. The unit capacitors are built in accordance to the present invention. The whole dummy capacitor border <u>is</u> connected to a terminal denoted G in figure 9. This is usually ground but can be used by the designer as an extra terminal of the capacitor array. All non-dummy unit capacitors have a common top terminal (denoted M [[if]] <u>in</u> Fig. 9). If we use the cross section from figure 9 and use a bi-dimensional approximation, we [[cam]] <u>can</u> calculate the capacitance between A and M and between B and M:

$C_{AM}=C_u+C_{nbt}$ and $C_{BM}=C_u+ 2 \times C_{nbt}$

Where C_u and C_{nbt} were defined above.

Please replace the paragraph beginning on page 13, line 8 with the following amended paragraph:

Figure 10 shows a possible solution to match the two array capacitances. The new dummy edge capacitor denoted E in figure 10 has three conductive regions defined in the middle layer (the one used for the top unit capacitor terminal). The right-most region denoted M is tied to the common terminal of the capacitor array denoted also M. The middle region is tied to terminal G (usually ground). The [[right]] left-most region (denoted F) can be left floating or tied to other terminal or even to ground. This part plays no electrical role. In the case in which matching due to non-uniform etching or other neighboring-related effects is good enough, this left part of the dummy edge capacitor can be even omitted.